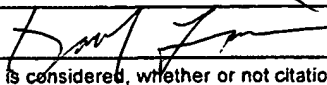


Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 244989US2S		SERIAL NO. New Application	
LIST OF REFERENCES CITED BY APPLICANT				APPLICANT Tsuneo INABA			
				FILING DATE Herewith		GROUP	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
DL	AA	5,946,227	08/31/99	Peter K. NAJI			
DL	AB	5,986,925	11/16/99	Peter K. NAJI, et al.			
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION		
					YES	NO	
DL	AO	2002-25245	01/25/02	Japan		x	
	AP						
	AQ						
	AR						
	AS						
	AT						
	AU						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
DL	AV	Roy SCHEUERLEIN, et al., "A 10ns Read and Write Non-Volatile Memory Array Using a Magnetic Tunnel Junction and FET Switch in each Cell", IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE, DIGEST OF TECHNICAL PAPERS, February 2000, 8 Pages					
DL	AW	M. DURLAM, et al., "NONVOLATILE RAM BASED ON MAGNETIC TUNNEL JUNCTION ELEMENTS", IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE, DIGEST OF TECHNICAL PAPERS, February 2000, 7 Pages					
DL	AX	Peter K. NAJI, et al., "A 256kb 3.0V 1T1MTJ Nonvolatile Magnetoresistive RAM", IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE, DIGEST OF TECHNICAL PAPERS, February 2001, 9 Pages					
DL	AY	Kouichi YAMADA, et al., "A Novel Sensing Scheme for a MRAM with a 5% MR Ratio", SYMPOSIUM ON VLSI CIRCUITS DIGEST OF TECHNICAL PAPERS, Session C12-1, June 2001, 2 Pages					
	AZ					<input type="checkbox"/> Additional References sheet(s) attached	
Examiner 					Date Considered 3/05		
*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							